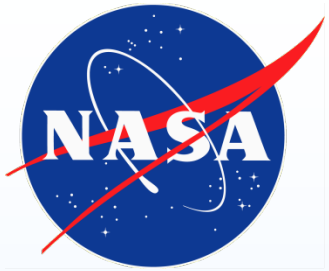

The NASA Electronic Parts and Packaging (NEPP) Program: Nonvolatile Memory Reliability Update

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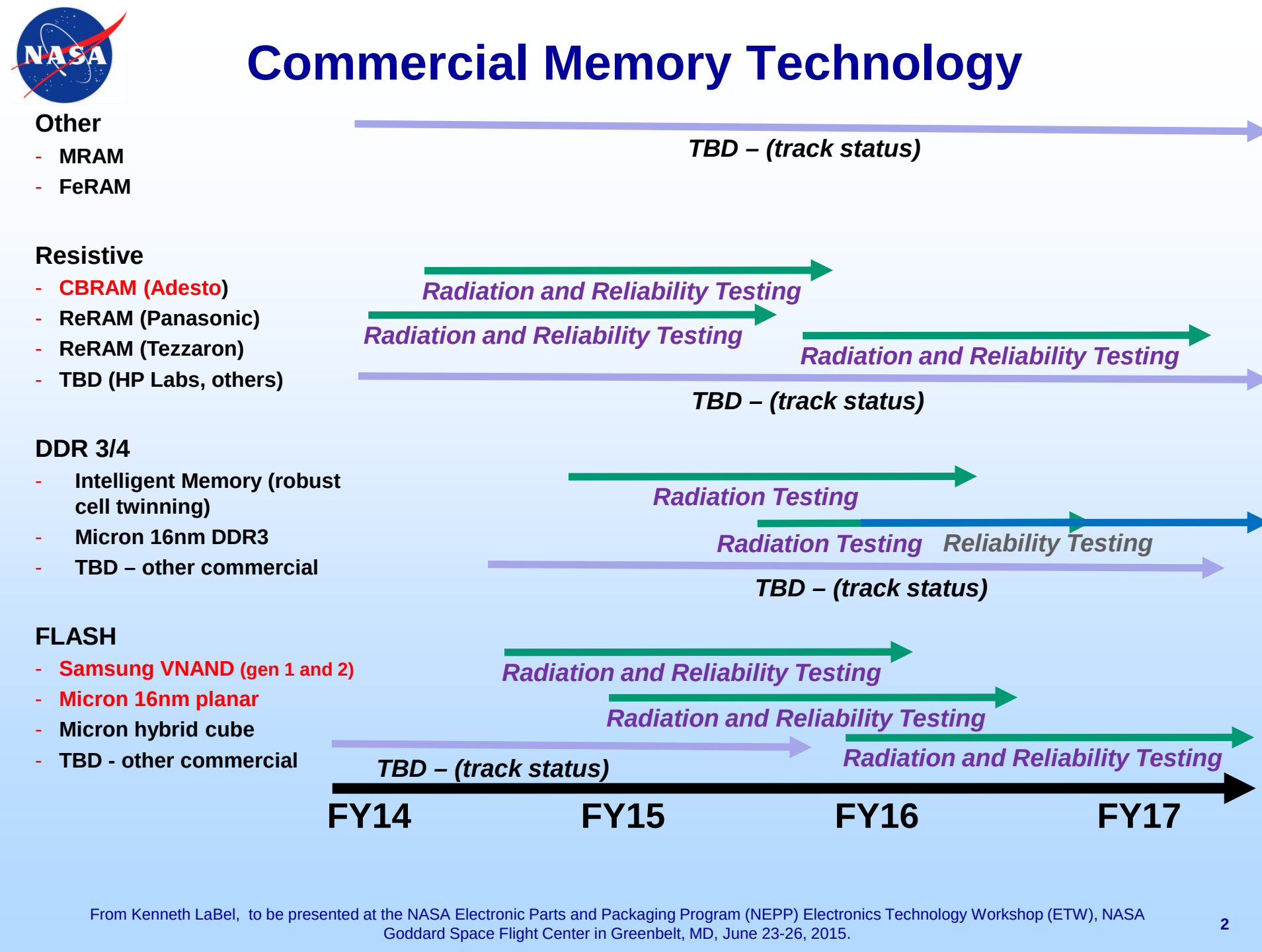
Acknowledgment:

This work was funded by NASA Office of Safety & Mission Assurance's (OSMA)

NASA Electronic Parts and Packaging Program (NEPP)

To be presented by Jean Yang-Scharlotta a at the NASA Electronic Parts and Packaging Program (NEPP) Electronics Technology Workshop (ETW), NASA Goddard Space Flight Center in Greenbelt, MD, June 23-26, 2015.

Commercial Memory Technology



Outline

- **Collaborations**
  - **GSFC- Dakai Chen and Carl Szabo**
  - **NSWC Crane- Matthew Kay and Austin Roach**
- **Motivation**
- **16nm Micron MLC Planar NAND**
- **50nm Samsung MLC VNAND**
  - **3D memory**
  - **New device and device architecture**
  - **Competitive new technology**
- **Adesto CBRAM (RRAM)**
  - **New resistive memory**
  - **Still maturing**

Motivation: Why Study Reliability for Advanced Nonvolatile Memories?

1. **Process Technology (Node) Driver is now Solid State Drive and not stand-alone NAND**
   - **first widely available mass produced parts at the 16nm node- Micron planar 16nm NAND**
   - **first widely available 3D memory part- Samsung VNAND**
   - **Lack of stand-alone NAND part availability is/will make it more difficult to study them**

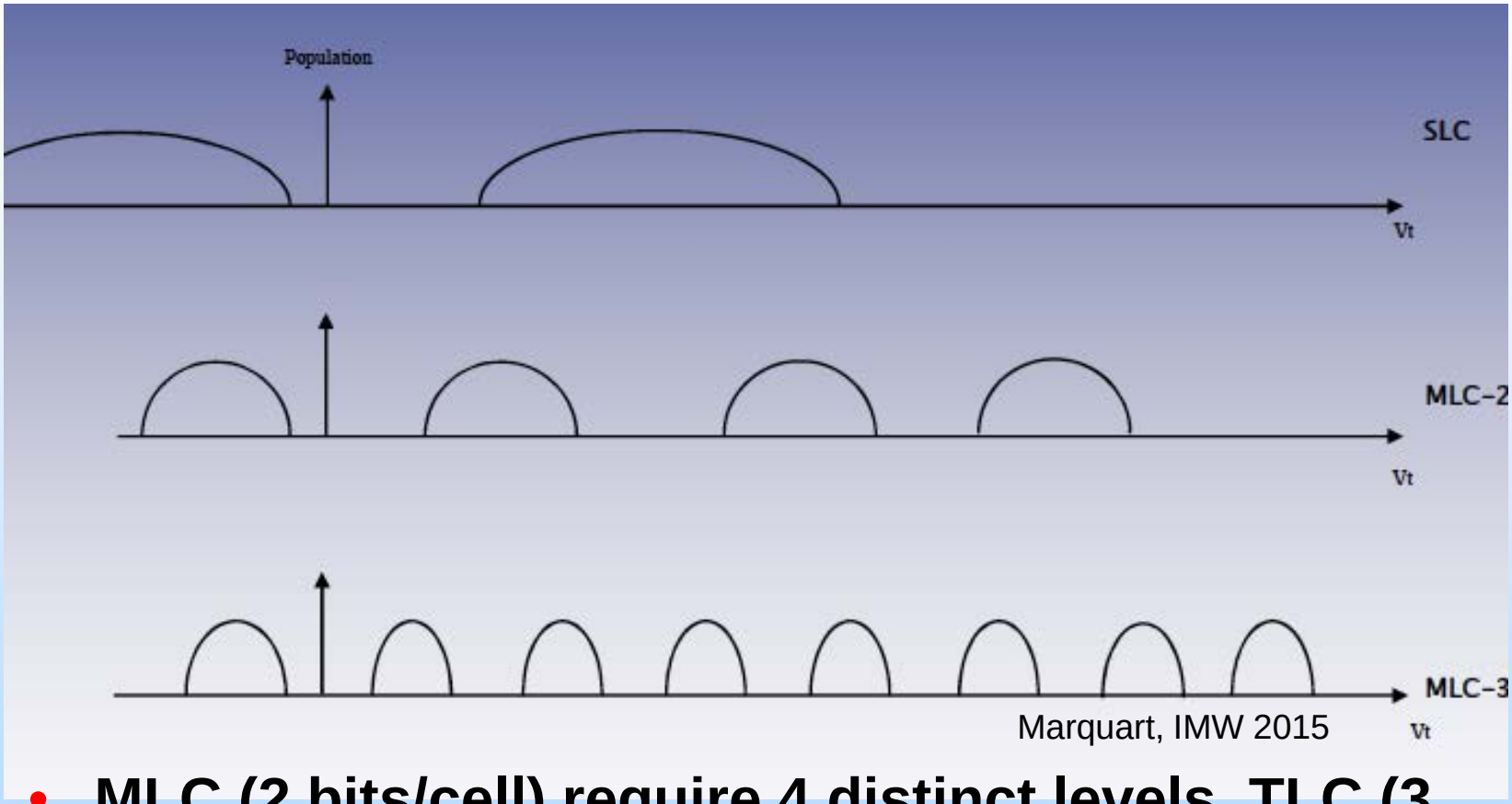
SSD Reliability Versus NAND Reliability

- SSD is a system while the NAND is a single part
- In an SSD, the NAND performance is carefully managed through a controller chip and a DRAM cache chip with error correction code, wear leveling techniques, spare blocks, data mapping and write buffering.
- SSD Key Metrics
  - Endurance is specified by total bytes written (TBW)
  - Uncorrectable bit error rate (not accessible to the user)
- NAND Key Metrics
  - Endurance is specified by Program/ Erase cycles for each block
  - Raw bit error rate
  - Data retention

Motivation: Why Study Reliability for Advanced Nonvolatile Memories?

2. **Nonvolatile Memory Complexity <u>Increased</u>**
   - **SLC (1bit/cell), MLC (2-bits/cell), and TLC (3-bits/cell)**
   - **3D architecture is now mainstream**
   - **Error correction code**
   - **Trend of NAND reliability requirements is toward more application specificity with scaling (less reliability margin)**
   - **emerging memories such as resistive memory may become better options for specific applications**

Vt Distributions for SLC (1bit/cell), MLC (2bits/cell), and TLC (3bits/cell)



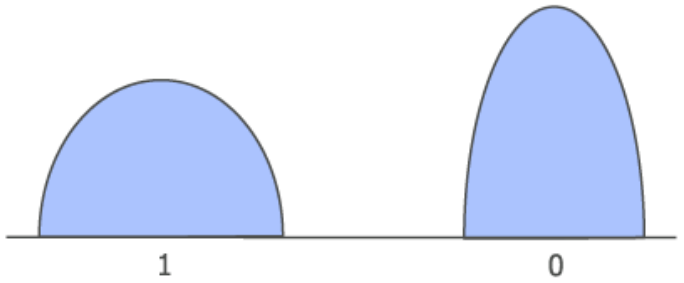
- **MLC (2 bits/cell) require 4 distinct levels, TLC (3 bits/cell) require 8 distinct levels**
- **larger Vt range and smaller margin.**

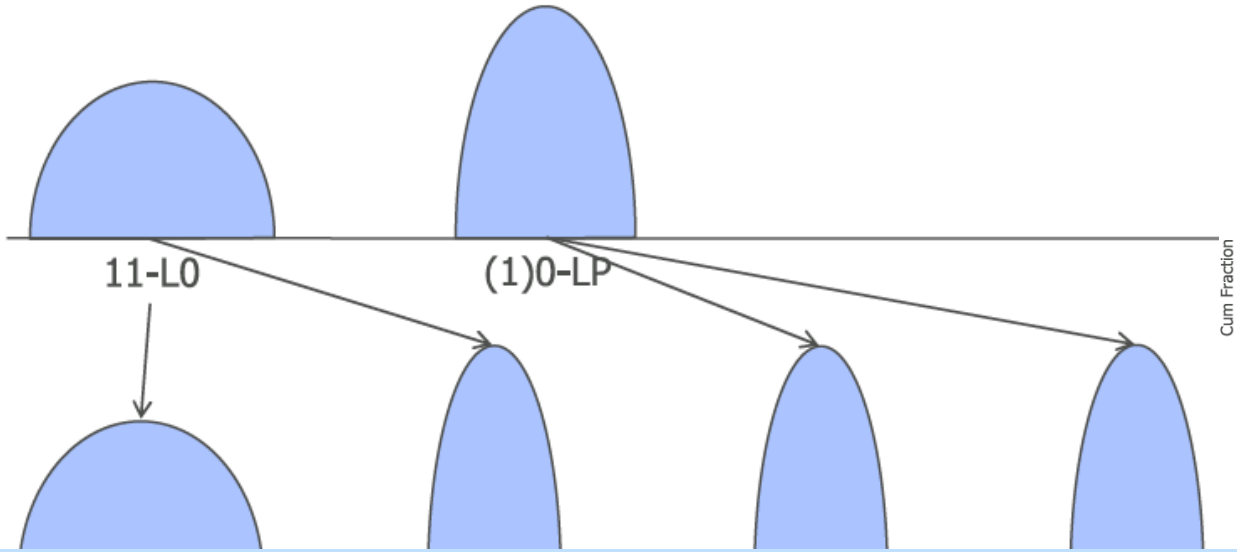
Multibit/cell Programming is Complex

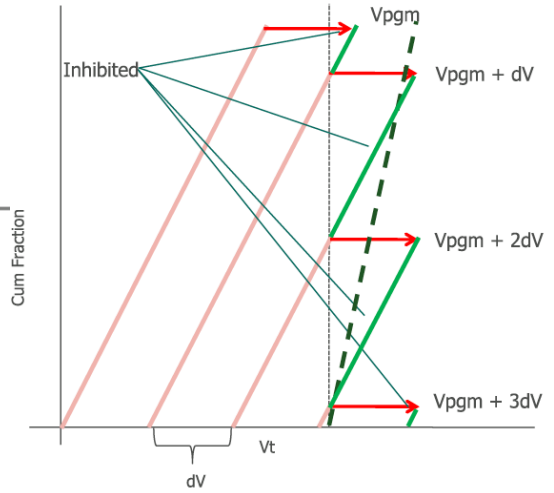
- Single programming operation
- 1 -> 0

MLC

- L0 ->LP
- LP->UP







–Marquart, IMW 2015

Multibit/cell programming require stepwise repeating programming and read sequences to get the tighter resulting distributions- more disturb

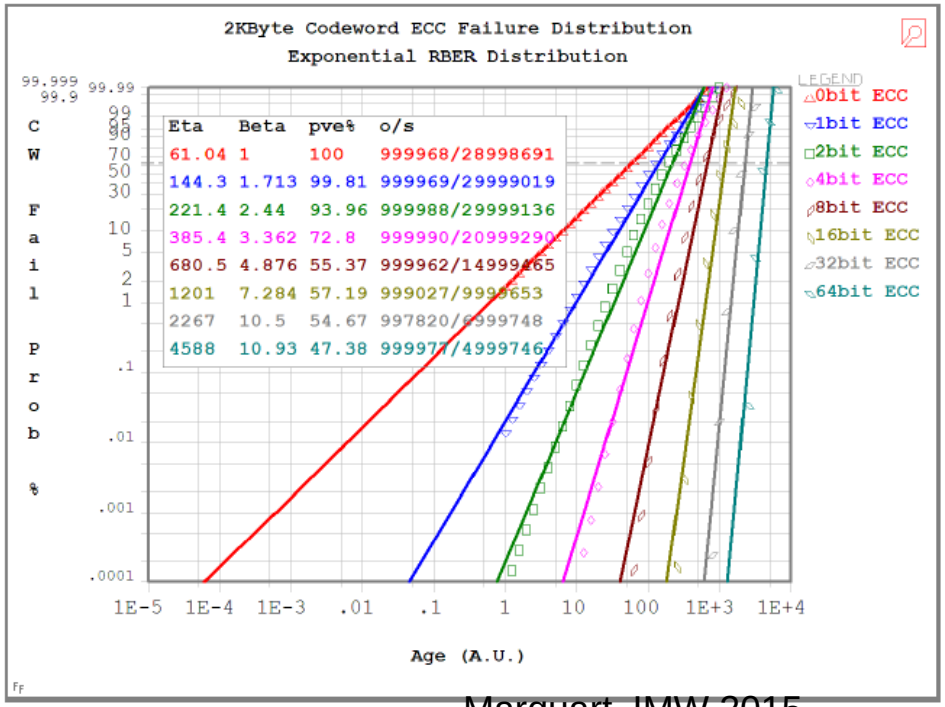
Error Correction Code

- **Error Correction Code allows for early life failures to not manifest to the users until near end of life**
- **Use of ECC masks failure rates and makes identification of mechanisms more difficult**

TABLE IV
ECC COMPARISON

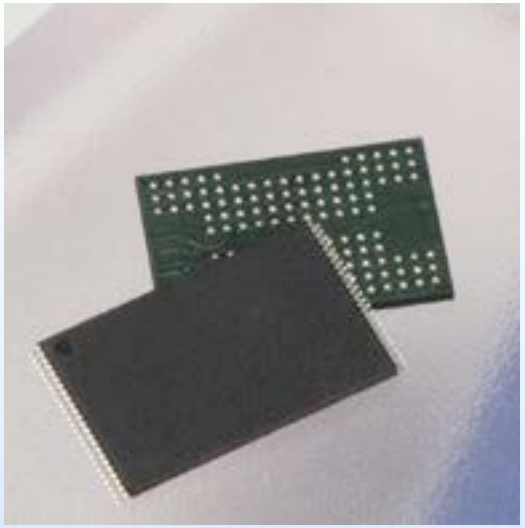
	Hamming code	RS	BCH	LDPC
Code	(4120, 4096)	(4240,4096)	(4304, 4096)	(8192, 4096)
Correctable error bits	1	8	16	4096
Storage overhead (%)	0.6	3.3	4.8	100 [9]
latency (μs)	34.5 [38]	44.3 [38]	41 [10]	41 [39]
Energy/byte (read/write) (pJ)	15/17 [38]	16/18 [38]	18/20 [11]	24/27 [9]

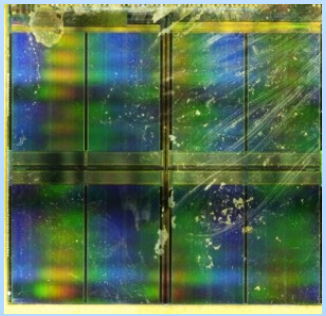
Xin Xu and H. Howie Huang, IEEE Trans. On Rel., 2015



–Marquart, IMW 2015

16nm Micron NAND Reliability Study

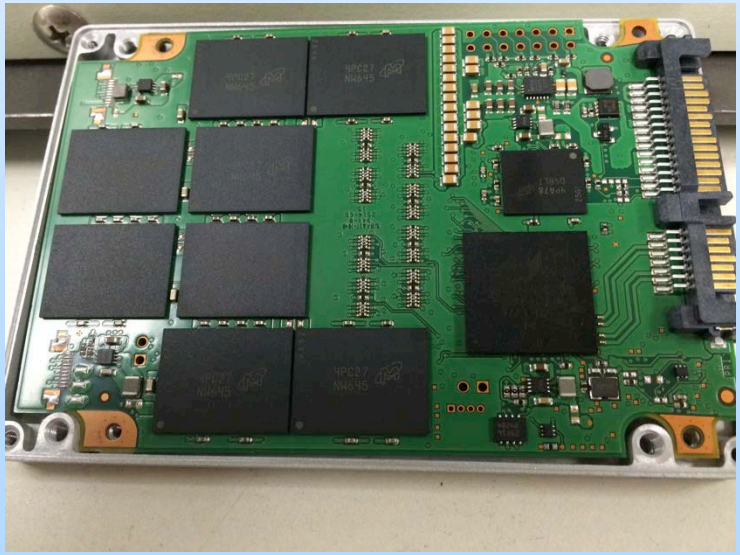




- **Micron 16um MLC NAND-**
- **We have both the SSD and the stand-alone NAND parts to compare reliability results**
- **NAND reliability test**
  - **Endurance: <u>3000</u> PROGRAM/ERASE cycles max**
    - **Begun to monitoring raw error rate change as a function of cycling.**
    - **Test planned for 25°, 70°C (data sheet) and further**
  - **Retention: JESD47 specified**
    - **Sliding retention scale (10 years for 300 cycles and 1 year for 3000 cycle count at max use temperature)**
    - **Low temperature post cycling retention test**
      - **For stress induced leakage current (SILC)**
    - **High temperature retention test for pre and post program cycled parts**
      - **for detrapping mechanism**
      - **Assume 1.1eV activation energy**

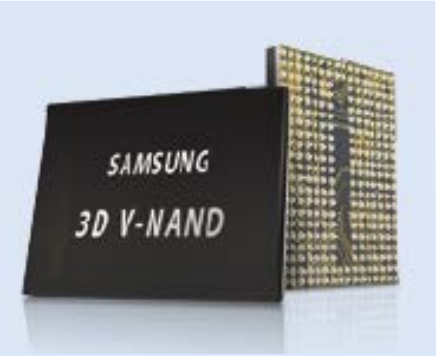
16nm Micron NAND SSD Reliability

- Micron 16nm MLC NAND in Crucial MX100 256GB SSD
  - Rate for 70°C operation and 85C storage
  - Capacity of 16GB per integrated circuit chip.
    - SSD reliability testing specified by JESD128
      - Endurance in total bytes written (TBW) = 72TB
        - for a 256GB capacity this translates to <300 program/erase cycles compared to 3000 for NAND
        - Actual program/erase cycles will be higher due to
          - Write Amplification
          - Wear leveling
      - Retention requirement is for 1 year at 30°C compared to 1 years at 70°C for 3000 cycle stressed NAND part
      - Uncorrectable bit error rate of $<10^{-15}$



Initial accelerated cycling endurance test shows 9% wear after writing 72TB in 3 weeks.

Samsung VNAND



- VNAND is only available in SSD format
- Samsung 850 PRO model of Solid State Drive contains 2nd generation 32 layer VNAND (3D-NAND) not available as stand-alone NAND
- Perform SSD level reliability characterization including data retention, endurance, wear leveling rate and temperature dependence utilizing 3rd party solid state storage analysis tools such as CAINE (Linux based), Iometer, while monitoring Self-Monitoring, Analysis and Reporting Technology (SMART) parameter .
- We need to test the smallest available SSD capacity since the entire drive has to be stressed
- Perform construction analysis and other destructive testing to evaluate cell and architecture difference from standard NAND

VNAND SSD Reliability Candidates

- **SAMSUNG 3D (2G MLC)- 850 PRO SSD 128GB**
  - **32 layer VNAND with 3 core MEX memory controller (ARM Cortex R4 400MHz) and 256MB LPDDR2 DRAM cache**
  - **Rated for 70C operation and 85C storage**
  - **Endurance rating of 150 TB of TBW**

- **SAMSUNG TLC planar NAND-840 SSD EVO 120GB (for comparison)**
  - **1x nm TLC NAND**
  - **Endurance rating of 75 TB of TBW**
  - **Same 3 core MEX memory controller and 256 MB DRAM cache (different execution)**
  - **Turbo Write uses a portion of the NAND as SLC buffer to accommodate TLC's slow write (3GB physical for 250GB)**

Initial accelerated cycling stress after 100TB showing 7 % wear for the VNAND and 30% wear for the planar TLC NAND

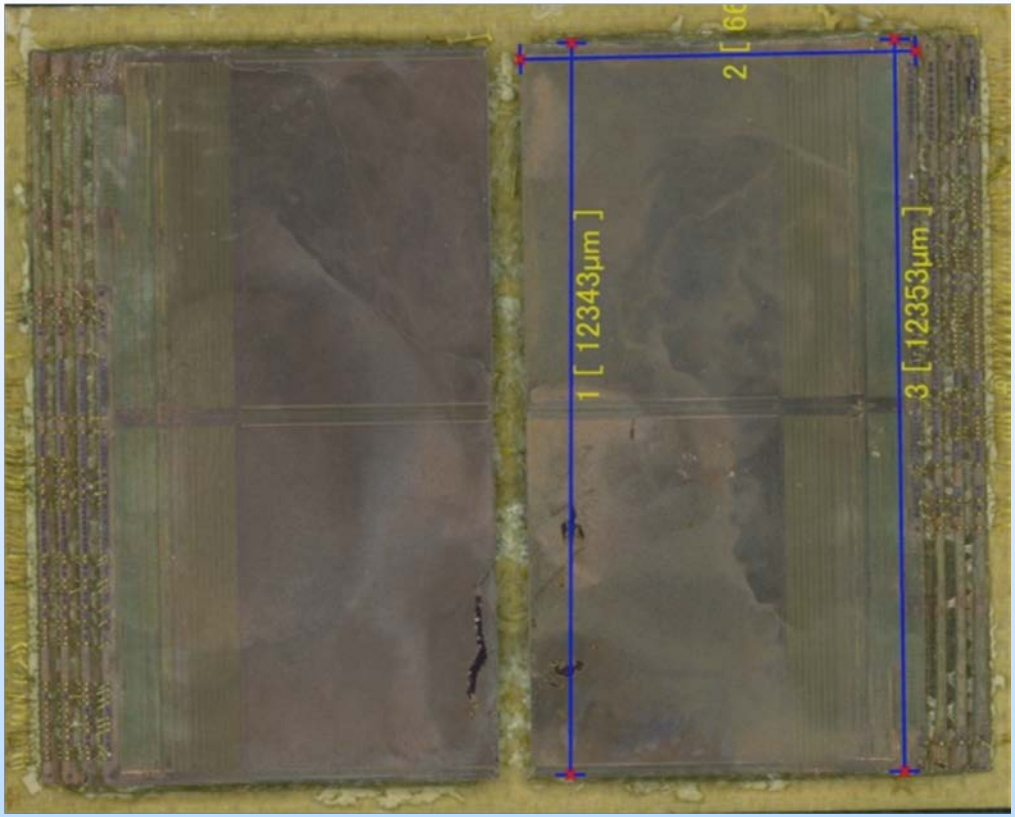
Continuing stress test for error data

2G VNAND Specifications

- 3D 86Gb MLC vertical NAND (V-NAND) flash memory
- 24-WL stacked layers Gen 1, 32-WL Gen 2, Gen 3 is TLC
- Good reliability and better power use than 2D NAND
  - 36MB/s + 35K endurance for high-end SSD :
  - 50MB/s + 3K endurance for mobile :
  - Capable of utilizing external high voltage source in SSD (12V) for power reduction (internal circuits may be designed for standard 3.2V or 1.8V Vcc)
    - Potentially better radiation tolerance by-reducing dependence on charge pumps
- Expected to continuing stacking more than next 5 generations

Park et al, ISSCC 2014

Gen 2 VNAND: Decapsulated“K9PRGY8S7M”



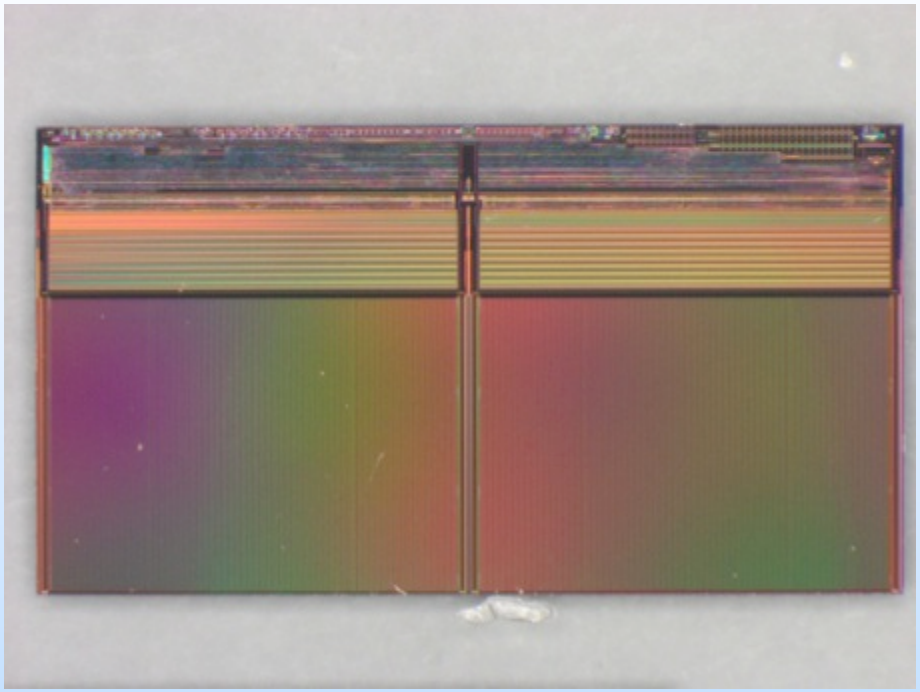
- 2x side by side stacks
- Each stack is 4 dice
- Each die is ~12350umx6670u
- For a total area of 82.4mm2

Samsung 850 Pro parts list for each capacity

Model:	Package code:	# of chips	RAW-capacity
128 GB	2x K9LPGYY8S1M (2)		
	2x K9HQGY8S5M (4)	12	129 gigabyte
256 GB	2x K9HQGY8S5M (4)		
	2x K9PRGY8S7M (8)	24	258 gigabyte
512 GB	4x K9HQGY8S5M (4)		
	4x K9PRGY8S7M (8)	48	516 gigabyte

- 2G VNAND is 86Gb per chip

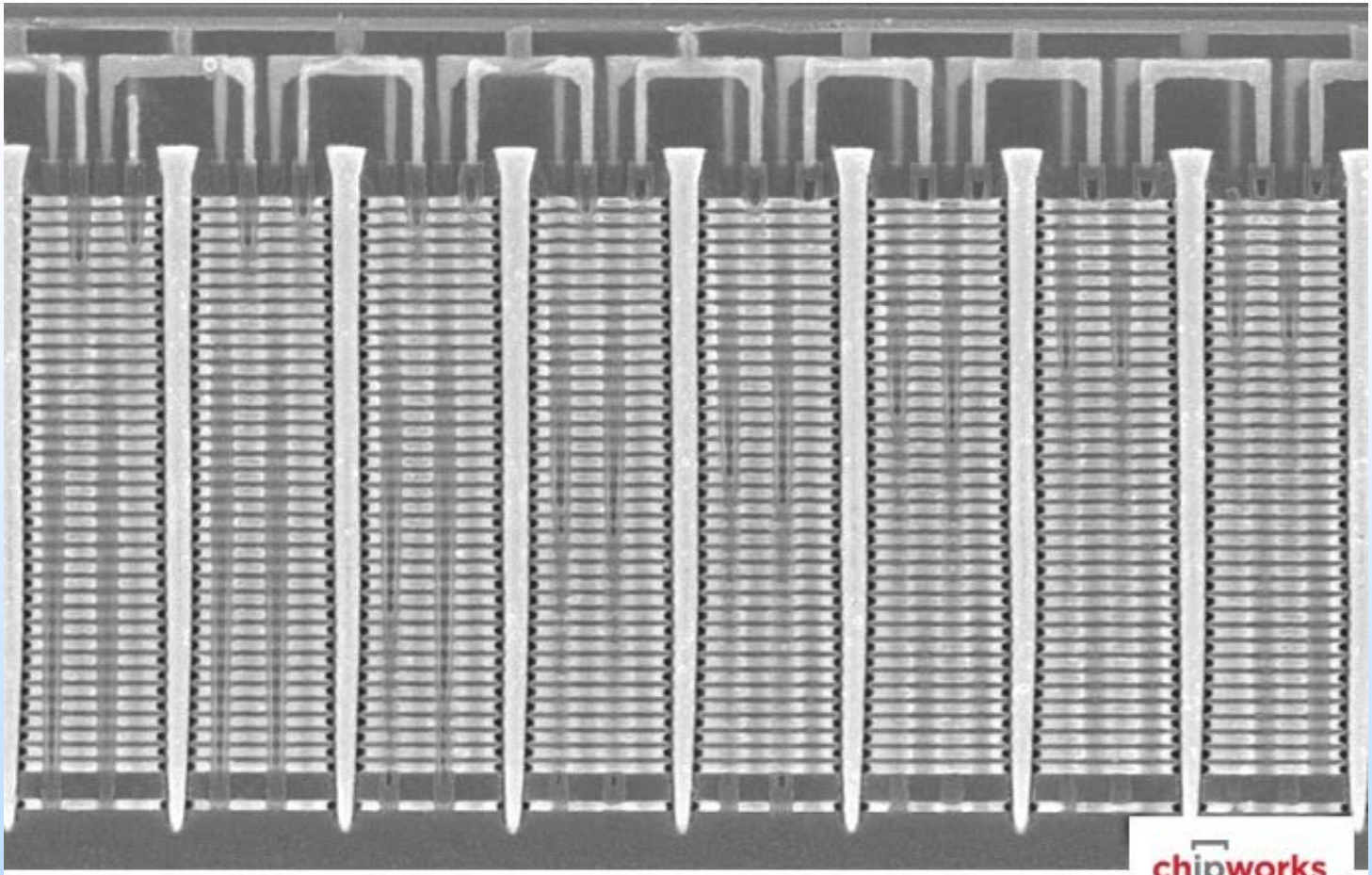
Close up of Die



Roach and Kay, NSWC Crane report 2-2015

- **All 4 die share the same die stamp**

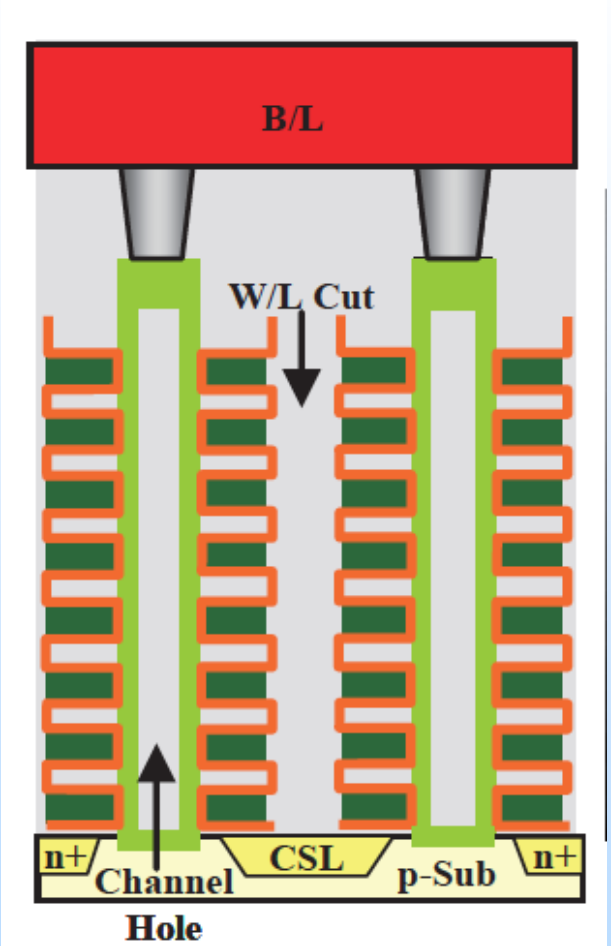
Close-up Image of 2G VNAND



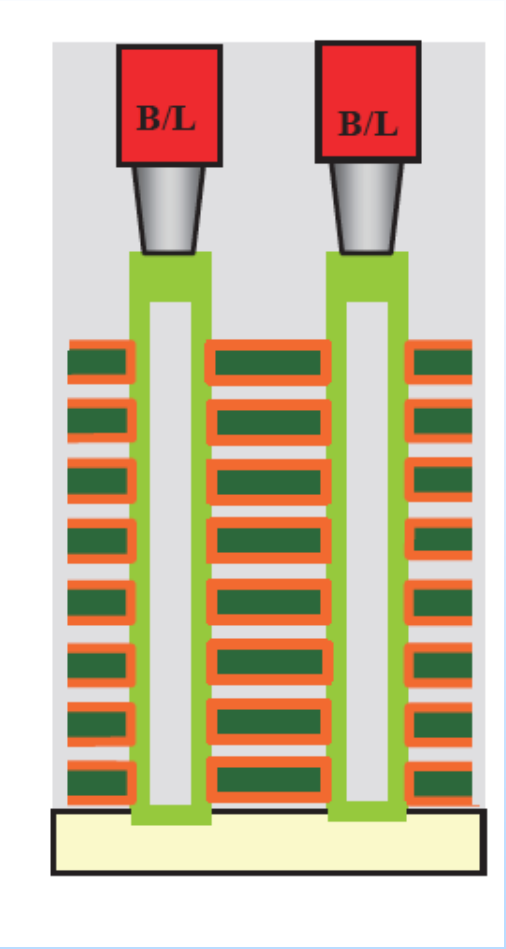
Close-up image of V-NAND flash array

- **32 wordline layers plus additional dummy word lines layers are expected based on Chipworks publication**

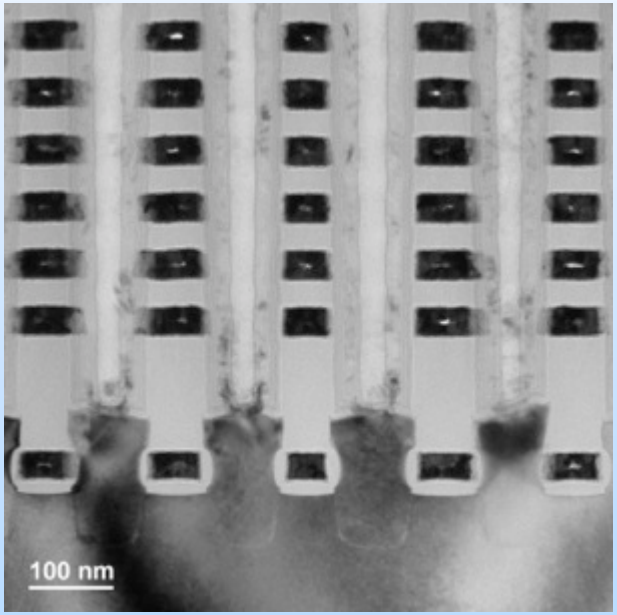
VNAND Array Details



X-direction



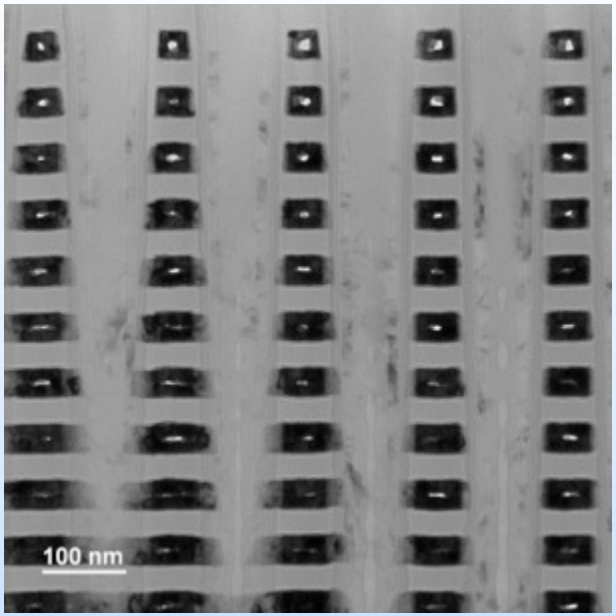
Y-direction



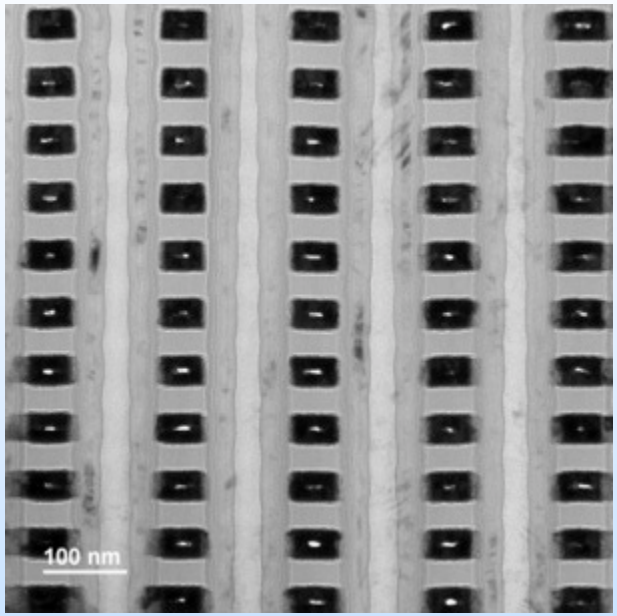
Y-direction (TEM)

Jang et al, VLSI, 2009

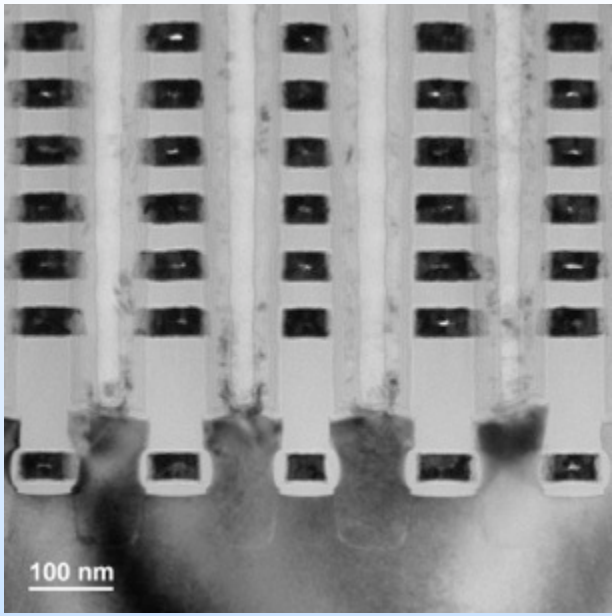
TEM Analysis of Gen 2 VNAND



top



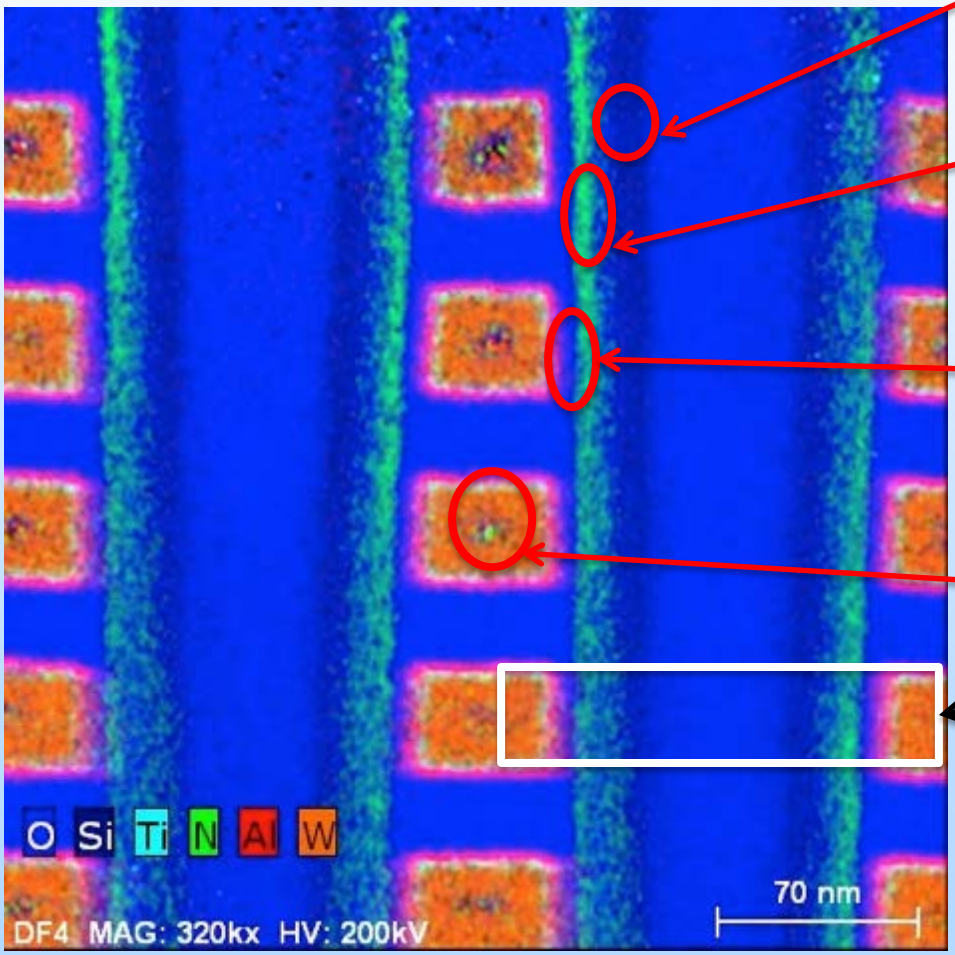
middle



bottom

- Gate (dark rectangles) is narrower at the top of the column probably to compensate for poly channel column taper
- Select transistor for each column is at the bottom

VNAND Bit Cell Structural Analysis



Dark Blue

Poly Si Channel ~100A

Green

Silicon Nitride Charge Trapping layer

~70A

Light Blue/pink

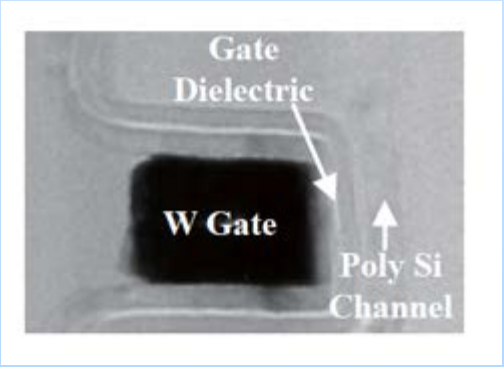
Blocking oxide layer (Al2O3?)

~70A

Orange

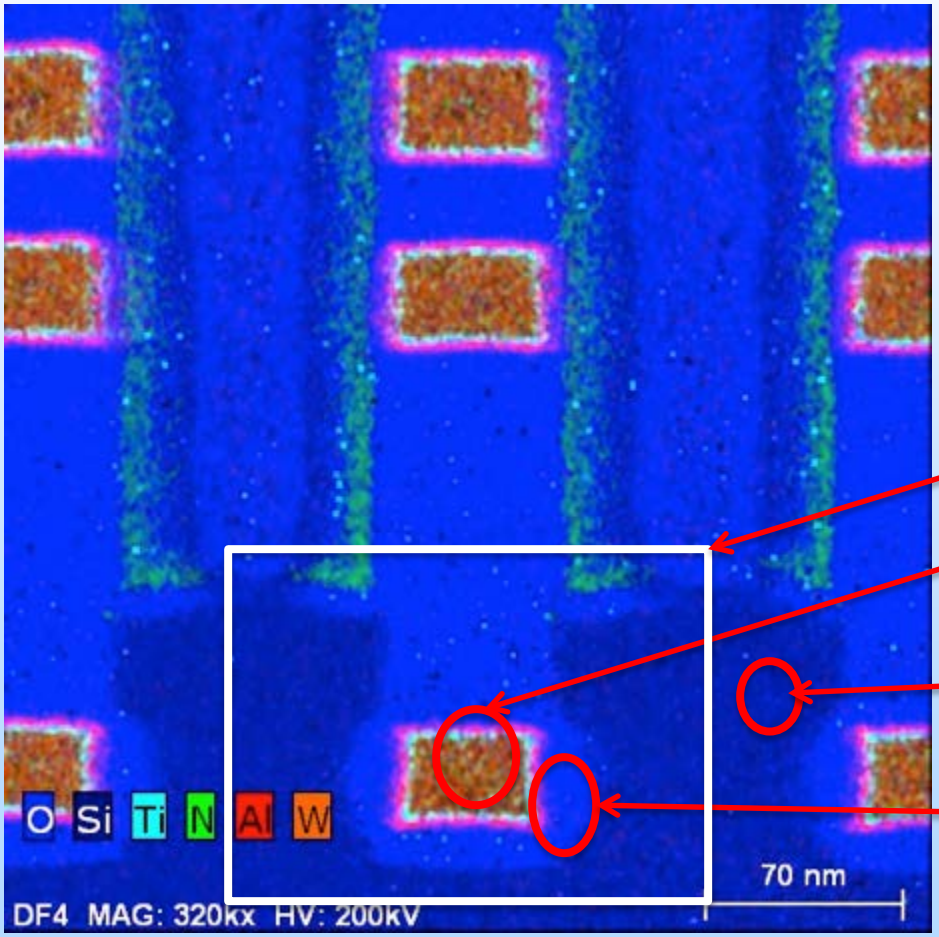
Tungsten gate

Bit Cell



Jang,VLSI 2009

Column Select Transistor Details
High Voltage (~15V curved channel)



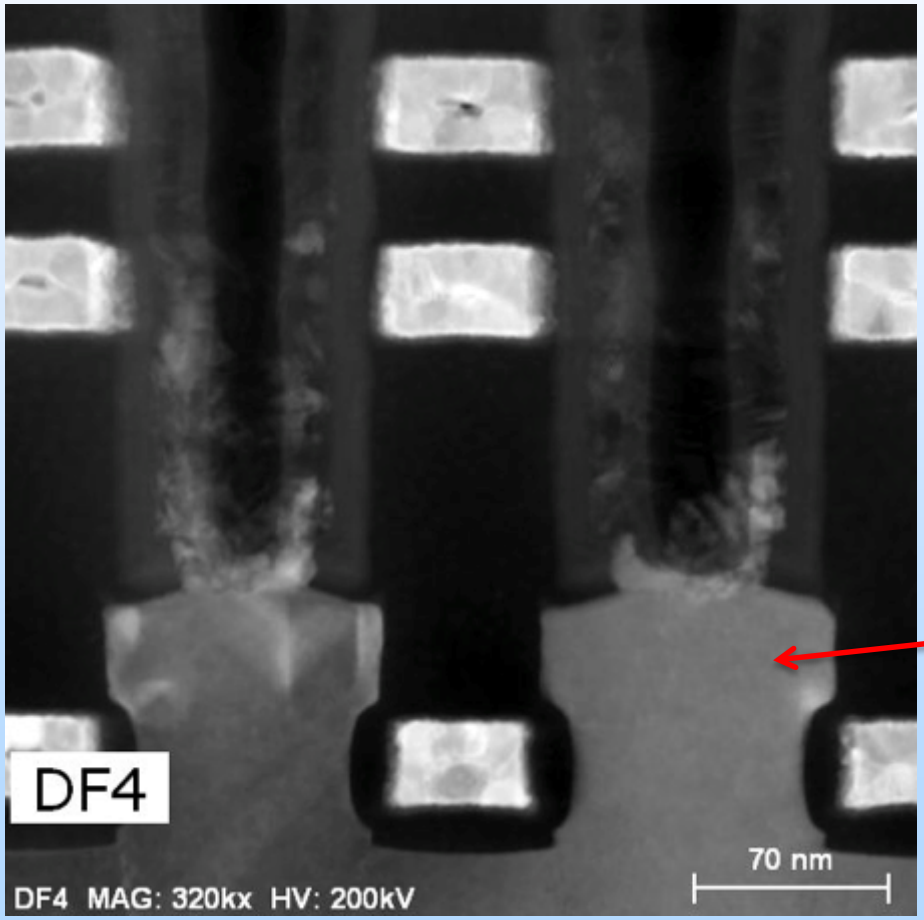
Select Transistor

Orange Tungsten Gate

Dark Blue Si Channel

Light Blue Gate Oxide ~200A

Dark Field TEM of Column Select Transistor



Typical feature size ~50nm

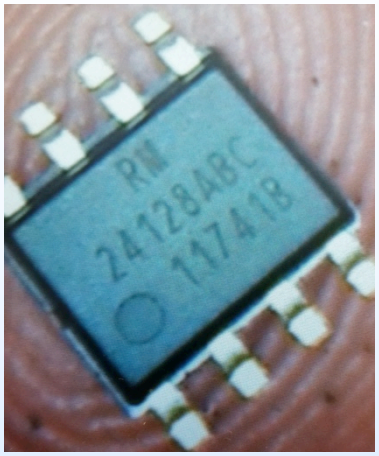
The 3D architecture utilizing ~50nm features competes well with 16nm planar

Column select transistor is formed in the silicon substrate

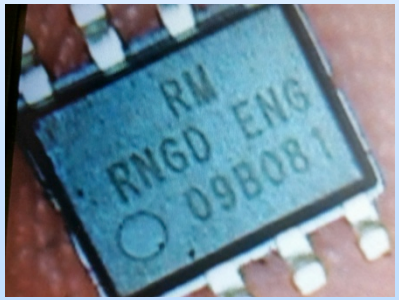
Adesto CBRAM Reliability Study

- Goals
  - This is an on-going evaluation of alternate NVM technologies in development.
  - Focus is the reliability and cell level analysis especially for new representative products in new technologies to look for unknown reliability concerns specific to space application
- Plans and Strategies
  - In depth study of the Adesto CBRAM technology based on Cu conductive bridge and compare fundamental reliability to the Panasonic TaOx resistive memory technology studied in FY14.
  - Reliability Study plans
    - Program cycling error rate: 25C, 85C and 125C operation
    - Endurance
    - Data Retention-activation energy calculation for lifetime
    - Combined effects of TID and data retention/endurance (resource permitting)

Adesto CBRAM Reliability Study



- RM24EP128A
  - 128Kbit 2.7V Minimum Sterilization-Tolerant Boot Memory
  - Rated for 0- 70C Operation and Storage -20 to 100C
  - 10 year data retention at 70C
  - 100 program cycles only for endurance
  - 200 kGy (20 MRad) of gamma ray and e-beam tolerant
  - Our initial data shows error rate increasing rapidly beyond the first few hundred cycles



- RM24EP64C
  - 64Kbit 2.7V Minimum Sterilization-Tolerant Non-volatile Serial Memory
  - Rated for 0- 70C Operation and Storage -20 to 100C
  - 10,000 program cycles endurance
  - 200 kGy (20 MRad) of gamma ray and e-beam tolerant
  - Our initial data shows error rate to be much more stable within the first few thousand cycles.
  - Will continue testing to determine temperature tolerance and activation energy for data loss.

QUESTIONS?